

Dautartas is even more explicit. Dautartas teaches in column 4 that a "hot wall reactor" be used. In particular, Dautartas states in relation to a hot wall reactor that:

it is important that the temperature in the deposition chamber be uniform because "cold spots" in the chamber can cause desorption of portions of the film. (emphasis original)

Similarly, it is believed that Utsumi teaches a hot wall system, and, at the least, does nothing to suggest the use of a cold wall system as now claimed in claims 20 and 52.

The present inventor discovered that the use of a cold wall system presents various advantages and benefits for the processes particularly described in the present application. For example, as stated in the specification on page 7, when using a cold wall chamber, reactants that are introduced into the chamber only react on the heated wafer, thus reducing the occurrence of any unwanted reactions and increasing the efficiency of the system. Cold wall systems have much faster heating and cooling rates than hot wall systems. Thus, in one embodiment, the fast heating rates can be matched to the time the reactants are in the system so that the reactions only take place during the heating cycle. Another key advantage to using a cold wall system is that purging of the reactants may be done using "cold" gasses in the chamber, which would create temperature variations in hot wall systems. In view of these advantages and benefits, it is believed that claims 20 and 52 patentably define over Utsumi, Nishizawa and Dautartas either alone or in combination.

In the Office Action, claim 50 was rejected was rejected under 35 USC § 102 in view of Nishizawa. Since Nishizawa discloses the formation of an aluminum phosphide

layer, it was asserted in the Office Action that this disclosure anticipates a solid layer comprising aluminum. In response, the "comprising" language has been removed so that claim 50 is specifically directed to the formation of an aluminum metal layer as opposed to a layer made from an aluminum compound. As such, it is believed that claim 50 is not anticipated by Nishizawa.

Finally, claim 51 was rejected under 35 USC § 103 in view of the combination of Nishizawa and Goodman. In response, claim 51 has been amended to remove reference to the formation of a nitride. As now drafted, claim 51 is directed to the formation of a solid layer comprising zirconium oxide, aluminum oxide, barium strontium titanate or a silicate. Since none of these materials are disclosed or suggested in either Nishizawa or Goodman, it is believed that claim 51 patentably defines over both references either alone or in combination.

In summary, it is believed that the present application is in complete condition for allowance. Should any issues remain after consideration of this amendment, however, then Examiner Markham is invited and encouraged to telephone the undersigned at his convenience.

Respectfully submitted by

DATE: October 2, 2002

DORITY & MANNING, P.A.

By: 

Timothy A. Cassidy

Reg: No. 38,024

P.O. Box 1449

Greenville, SC 29602-1449

(864) 271-1592 (Tel.)

(864) 233-7342 (Fax)

## APPENDIX A

20. A process for forming layers in electronic devices comprising the steps of:  
providing a reaction chamber, the reaction chamber comprising a cold wall chamber;

placing a semiconductor wafer in said reaction chamber;

heating said semiconductor wafer with a thermal heating device placed adjacent to said wafer;

pulsing a precursor fluid into said reaction chamber, said precursor fluid forming a solid layer on said semiconductor wafer;

thereafter exposing said solid layer to light energy in said reaction chamber; and

wherein between each pulse of said precursor fluid, (i) said reaction chamber is purged by flowing an inert gas through said reaction chamber in order to substantially remove any said precursor fluid not converted into a solid, and (ii) said solid layer is exposed to said light energy.

50. A process for forming layers in electronic devices comprising the steps of:  
providing a reaction chamber;

placing a semiconductor wafer in said reaction chamber;

heating said semiconductor wafer with a thermal heating device placed adjacent to said wafer;

pulsing a precursor fluid into said reaction chamber, said precursor fluid forming a solid layer on said semiconductor wafer, wherein said solid layer [comprises] is a material selected from the group consisting of tungsten, tungsten nitride, tantalum nitride, titanium nitride, copper, aluminum, ruthenium oxide, iridium oxide, and silver; and

thereafter exposing said solid layer to light energy in said reaction chamber;

wherein said precursor fluid is substantially exhausted and removed from said reaction chamber and said solid layer is exposed to said light energy in between each pulse of said precursor fluid.

51. A process for forming layers in electronic devices comprising the steps of:

- providing a reaction chamber;
- placing a semiconductor wafer in said reaction chamber;
- heating said semiconductor wafer with a thermal heating device placed adjacent to said wafer;
- pulsing a precursor fluid into said reaction chamber, said precursor fluid forming a solid layer on said semiconductor wafer, wherein said solid layer comprises a material selected from the group consisting of zirconium oxide, aluminum oxide, [a nitride,] barium strontium titanate and a silicate; and
- thereafter exposing said solid layer to light energy in said reaction chamber;

wherein said precursor fluid is substantially exhausted and removed from said reaction chamber and said solid layer is exposed to said light energy in between each pulse of said precursor fluid.